IN THE SPECIFICATION

Kindly replace the following paragraphs beginning on page 14, line 5 and ending on page 16 line 3 with the following paragraphs:

Figure 5 is a diagram illustrating an exemplary embodiment of a storage system 70. In the exemplary embodiment, storage system 70 includes a control system 132. Control system 132 includes firmware 134 and microcontroller 136. The control system 132 illustrated in Figure 5 is another embodiment of control system 32 illustrated in Figure 1, and as such, the operation of control system 32 and 132 is also illustrated and described in Figure 1. Control system 132 is configured to periodically obtain parametric values from magnetic memory cells 14 in the magnetic memory storage devices ~~74~~ 74a and 74b and generate, using the parametric values, one or more compressed fault maps or error detection code results. The compressed fault maps or error detection code results are compared to one or more previous compressed fault maps or error detection code results, an indication is provided at 138 if there are differences.

Control system 132 is coupled via lines ~~72~~ 72a and 72b to magnetic memory storage devices ~~74~~ 74a and 74b. Each magnetic memory storage device 74a and 74b has four arrays 12a, 12b, 12c and 12d of magnetic memory cells 14. In other embodiments, each magnetic memory storage device ~~74~~ 74a and 74b can include any suitable number of arrays 12. In other embodiments, each magnetic memory storage device ~~74~~ 74a and 74b can include any suitable number of magnetic memories 10.

In the exemplary embodiment, the arrays 12 are independently addressable and are arranged to form a stack consisting of arrays 12a, 12b, 12c and 12d. Although only two

memory storage devices 74 74a and 74b or stacks 74 74a and 74b of array 12 are illustrated,

any suitable number of stacks 74 74a and 74b can be used.

In one exemplary embodiment, the memory storage devices 74 74a and 74b are

arranged to form a 20 by 16 arrangement of stacks 74 74a and 74b, where each stack 74 74a

and 74b includes four arrays 12. Each array 12 includes an array of 1024 by 1024 magnetic

memory cells 14 or bits. In the exemplary embodiment, the storage system 70 has a storage

capacity of 1,280 M bits. This storage capacity can be viewed as a logical sequence of

262,144 sectors, where each sector contains 640 bytes. In one embodiment, within each

sector, 512 bytes are available for storage of user data, and 128 bytes are reserved for error

correction codes. In other embodiments, other arrangements of memory storage devices 74

74a and 74b can be used. In these other embodiments, each memory storage device 74 74a

and 74b includes a suitable number of arrays 12.

Figure 6 is a diagram illustrating an exemplary embodiment of an unsorted fault map

82, a sorted fault map 84 and a fault map signature 86. The fault maps 82 and 84 and the

fault map signature 86 are illustrated at 80.

In the exemplary embodiment, the memory storage devices 74 74a and 74b are

arranged to form a 20 by 16 arrangement of stacks 74 74a and 74b, where each stack 74 74a

and 74b includes four arrays 12. Each array 12 includes an array of 1024 by 1024 magnetic

memory cells 14 or bits.

In the exemplary embodiment, an uncompressed fault map which is an unsorted fault

map 82 includes for each fault, a fault type and a fault location or address of the magnetic

memory cell 14 having the fault. The fault type is represented as a two bit binary number

designating either an open-bit failure, a shorted-bit failure, an indeterminate state failure

(single failed bit) or a half-select failure. The fault location is represented as a 31 bit binary number which includes a stack ~~74~~ 74a and 74b x coordinate (5 bits), a stack ~~74~~ 74a and 74b y coordinate (4 bits), an array 12 location in the stack ~~74~~ 74a and 74b (2 bits), an array 12 x-coordinate or column line 18 location (10 bits), and an array 12 y-coordinate or row line 16 location (10 bits). Each fault is represented by 33 bit binary number formed by concatenating the fault type (2 bits) with the location of the fault (31 bits). Because compressed fault maps are compared while uncompressed fault maps (e.g. the unsorted or sorted fault maps) are not compared, in other embodiments the number of bits used in the uncompressed fault maps can be any suitable number.

The unsorted fault map 82 has a first fault illustrated as "01 02 09 03 02 0c 00 de". This fault has a type of (01) which can be, for example, a shorted bit failure. The coordinates of stack ~~74~~ 74a and 74b in the 20 by 16 arrangement is (x=2, y=9). The location of the layer or array 12 within the stack ~~74~~ 74a and 74b is (3) which can be, for example, array 12c (see also, Figure 5). ~~The coordinates of the fault within the stack 76 is (x = 524, y = 222).~~ This information is encoded into an 8 byte sequence as "01 02 09 03 02 0c 00 de" where 524 decimal equals 020c hex, and 222 decimal equals 00de hex. In other embodiments, the fault type is not included in the unsorted fault map.